

10/801962

Sheet 1 of 1

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 01701.00204	SERIAL NUMBER Div. of 10/607,301
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LP	6,459,118 B1	10/02	Kang			
	6,320,783 B1	11/01	Kang et al.			
	6,088,286	7/00	Yamauchi et al.			
	5,903,492	5/11/99	Takashima			
	5,894,447 A	04/99	Takashima			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

LP	K. Noda et al., "A Boosted Dual Word-line Decoding Scheme for 256Mb DRAMs" Symposium on VLSI Circuits Digest of Technical Papers; pp. 112-113; 1992.
LP	M. Nakamura et al., "A 29ns 64Mb DRAM with Hierarchical Array Architecture" IEEE International Solid-State Circuits Conference, pp. 246-247, 1995.

EXAMINER	<i>pham</i>	DATE CONSIDERED	06/23/2004
EXAMINER/Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.			